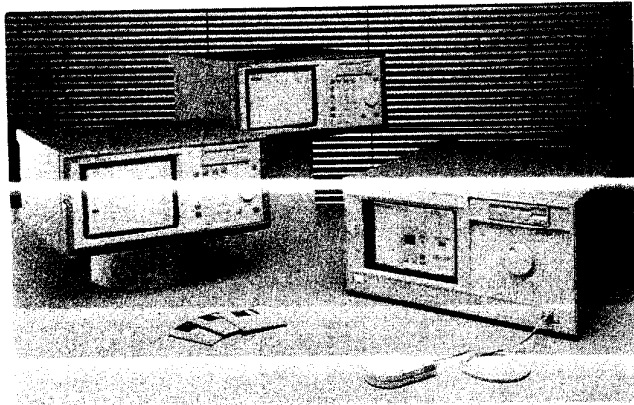# LOGIC ANALYZERS
State, Timing, Analog, and Stimulus/Response Analysis
Model 1631A/D, 1650A, 1651A, 16500A, 16510A, 16515A/16A, 16520A/21A, 16530A/31A

Memory	1 Kbit/channel	1 Kbit/channels
Microprocessor support	Today's most popular 8-, 16-, and 32-bit microprocessors	Today's most popular 8-bit microprocessors
Price	$7800	$3900

	LOGIC ANALYSIS	1 GHz TIMING	PATTERN GENERATION	DIGITIZING OSCILLOSCOPE
Module	HP 16510A**	HP 16515A/ HP 16516A	HP 16520A/ HP 16521A	HP 16530A/ HP 16531A
Channels Per Card	80	16	12/48	2
Maximum Channels Per System	400	80	204	8
Memory Depth	1K	8K	4K	4K
Maximum Rate	25 MHz State 100 MHz Timing	1 GHz Timing	50 Mbits/s	400 Msamples/s 100 MHz Bandwidth
PRICE	$5200	$7800/ $6500	$3700/ $4000	$1500/ $4000

**The HP 16510A has the same capabilities as the HP 1650A and contains 5 of HP's Logic Analyzer-on-a-Chip.

Introducing HP's New Family of Logic Analyzers and Logic Analysis Systems . . .

Performance
- Up to 400 channels of general-purpose logic analysis.
- Up to 80 channels of 1 GHz timing analysis.
- Up to 204 channels of 50 Mbit/s pattern generation.
- Up to 8 channels of 400 Msample/s digitizing oscilloscope capability.

Ease-of-use
- Save time and avoid errors using the HP 16500A's color touch screen or mouse.
- Make measurements quickly with the HP 1650A/1651A's simplified user-interface.
- Give the knob a spin to change values quickly or move measurement markers.

Value
- Rely on HP's traditional reliability and quality for low cost-of-ownership.
- With Option W30, get 3 year protection for your HP 1650A/1651A/16500A.
- These products come with a one year standard warranty. Option W30 adds two additional years of return-to-HP service.
- Get assistance when and where you need it with HP's worldwide sales and support organization.

Setup Convenience
- Set up your digitizing oscilloscope or your timing analyzer with push button ease using HP's Auto-Scale.
- Connect to your circuit with new lightweight passive probes and flexible cables.
- Hook up quickly to today's most popular 8-, 16-, and 32-bit microprocessors with HP's preprocessors.
- Store and recall configurations from built-in disc drives for fast setup.

	HP 1650A	HP 1651A
Timing	100 MHz on ALL 80 channels	100 MHz on ALL 32 channels
State	25 MHz on ALL 80 channels	25 MHz on ALL 32 channels

Simple, Yet Does the job . . . and More
- Lengthen your timing window with transitional timing on ALL channels.
- Capture elusive glitches with glitch detection on ALL channels.
- Configure the HP 1650A/1651A in four ways: one state analyzer, one timing analyzers, or one state and one timing analyzer.
- Store setups and measurement results with the built-in disc drive for fast recall or permanent records.
- Generate report-quality documentation with push button ease.
- Program the HP 1650A/1651A with easily understood commands through the built-in RS-232C interface.

Fits Where You Need It . . . Goes Where You Want It
- Compact: With its small footprint, the HP 1650A/1651A fits easily on your bench, within the same field of vision as what you're working on.
- Portable: At only 22 lbs., the HP 1650A/1651A can be easily carried with its built-in handle or the HP 1540-1066 soft carrying case.
- One Piece: Keep everything together, in one place; the probes and cables fit conveniently into the pouch attached to the top of the instrument.

### Solutions for individual Requirements and Group Needs
- Customize your own system by adding cards to the HP 16500A's five card slots.
- Make time-correlated measurements between cards using the HP 16500A's Intermodule Bus.
- Compare measurement data from hardware with design simulation data using the HP Electronic Design System and the HP 16500A Logic Analysis System.
- Program the HP 16500A with easily understood commands through HP-IB or RS-232C built-in interfaces.
- Store setups and measurement results in either of two built-in disc drives for fast recall or permanent record.
- Generate report-quality documentation with push button ease.

Today's Best Value in General-purpose Logic Analyzers
Model 1650A, 1651A

- HP 1650A-80 channels, HP 1651A-32 channels of 25 MHz state or 100 MHz timing
- Transitional timing for deep effective memory

- Supports most popular 8-, 16-, and 32-bit microprocessors
- Lightweight passive probing
- Simultaneous state/state, simultaneous state/timing

HP 1650A **NEW**
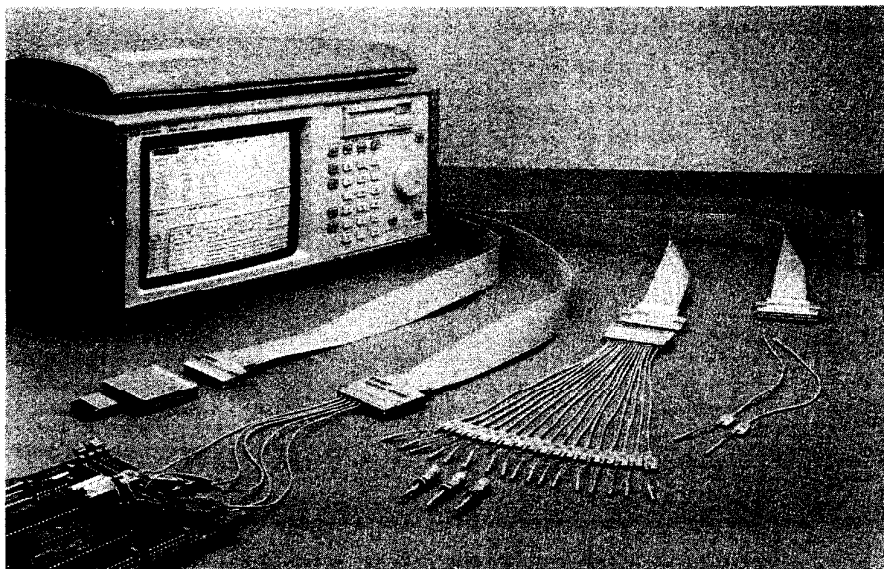
Hook Up Quickly and Reliably to Your Circuit

HP's new passive probes are small and lightweight. With an input impedance at the probe tip of 100k ohms in parallel with 8 pF, these probes won't load down your circuit. Individual probes and cables can be removed when they get in the way. Additionally, the HP 01650-63201 Terminating Adaptor enables you to connect your logic analyzer directly to PC boards with 2x10, 0.1" center connectors.

Overlap all data channels on the display to measure when all lines are stable.

Extend the Memory of Your Timing Analyzer with Transitional Timing

Traditionally, a timing analyzer samples the input channels based on its own internal clock and then stores every sample in memory. The HP 1650A/1651A/16510A store data only when there is a transition, thus avoiding redundant data. This effectively extends the memory by lengthening the time covered by an acquisition. The timing analyzer samples at full speed so that events that are seconds or even minutes apart are captured with 10 ns resolution.

Debug Quickly with up to 80 Channels

The HP 1650A/1651A/16510A's 5 ns minimum glitch capture on all channels looks for activity between samples. Pattern search helps you to find a specific event quickly. Overlay mode places several timing signals on one display line, so that you can see where timing violations occur. Infinite persistence shows the changes in waveforms during repetitive acquisitions. When more channels means spending less time to find the problem, use up to 80 channels.
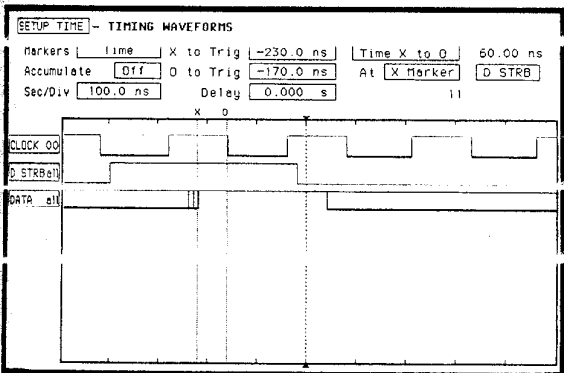
Capture the Data You Want to See

Trigger on a pattern across the full number of channels. Or you can qualify a pattern by specifying a duration, glitch, or edge. Specify a pattern duration to capture error conditions indicated by a pattern that exceeds a specified limit. When you need to see what is happening around a troublesome glitch or hardware interrupt signal, use glitch or edge triggering.

Focus on the Information You Need

The HP 1650A/1651A/16510A's complex state triggering filters out unnecessary data and provides a listing of the crucial data:

- 3 clock inputs and 4 clock qualifiers allow your system to determine when the analyzer takes a sample.
- Storage qualification allows you to specify which states are stored in memory.
- 8 sequence levels determine the sequence of states required for trigger and help you to focus on a specific area of code execution.
- 8 pattern recognizers, 1 range recognizer or logical combinations of these are used to identify states that are stored.
- Tagging keeps track of the amount of time or the number of states between stored states.
- Enable/Disable can be used to restrict storage to the activity of a specific routine.
- Prestore stores two qualified states that precede the states that are normally stored.

Model 1650A, 1651A

```
6809 STATE - STATE LISTING          (Specify Stop Measurement)
Markers   [ Pattern ]  Find [x-pattern]  [  ] from [ Trigger ]
Pattern > [ 0039 ]

Label  >  ADDR   6809/6809E Mnemonic              STAT
Base   >  Hex    hex                             Symbol
+0120    F80A   LDY  #1000                       OPCODE
+0121    F80B    0E  program read                PROGRAM
+0122    F80C    10  program read                PROGRAM
+0123    F80D    00  program read                PROGRAM
+0124    F80E   LDU  #1000                        OPCODE
+0125    F80F    10  program read                PROGRAM
+0126    F810    00  program read                PROGRAM
+0127    F811   TFR  B,DP                         OPCODE
+0128    F812    9b  program read                PROGRAM
+0129    F813   ABX                               OPCODE
+0130    F814   ADCA  #55                         OPCODE
+0131    F815    55  program read                PROGRAM
+0132    F816   ADCA  <0039                       OPCODE
+0133    F817    39  program read                DATA
x+0134   0039    FF  data read                   DATA
+0135    F818   ADCA  1000                        OPCODE
```

```
MACH A  - STATE LISTING  (Invasm)   (Specify Stop Measurement)
Markers   [ Pattern ]  Find [x-pattern]  [  ] from [ Trigger ]

Label  >  ADDR   80386 Mnemonic                      STA
Base   >  Hex    hex                                 Sym
0 +0004  FFFFFFF8  JMP FFF0H:0024H                 CODE RD
+0005    FFFFFFFA  xxxxF000H  code read            CODE RD
+0006    FFFFFFFC  ADD [DX)(SI],AL                 CODE RD
+0007    FFFFFFFE  ADD  no operand                 CODE RD
x +0008  000FFF24  CLI                             CODE RD
          MOV SI,#0000H
+0009    000FFF26  xxxx0000H  code read            CODE RD
+0010    000FFF28  MOV DI,#0100H                   CODE RD
+0011    000FFF2A  MOV CX,#0018H                   CODE RD
+0012    000FFF2C  xxxx0018H  code read            CODE RD
+0013    000FFF2E  CLD                             CODE RD
          MOV AX,#  no operand
+0014    000FFF24  CLI                             CODE RD
+0015    000FFF26  xxxx0000H  code read            CODE RD
+0016    000FFF28  MOV DI,#0100H                   CODE RD
```

Motorola 6809 state listing and Intel 80386 state listing, both with inverse assembly.

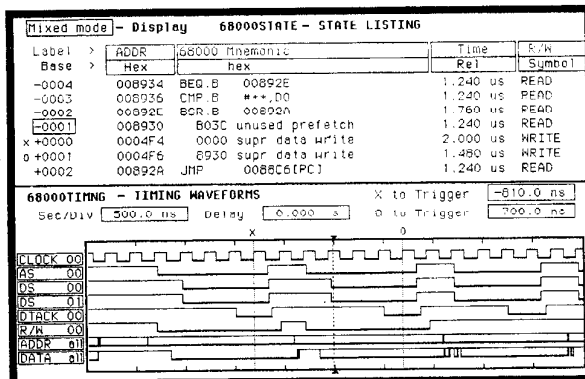### Debug Designs that Use Today's Most Popular Microprocessors

HP's preprocessors tailor the HP 1650A/1651A/16510A to microprocessors from Intel, Motorola, Zilog, and National. These preprocessors simplify hookup by plugging directly into the CPU's socket. Companion software converts the acquired state data into microprocessor mnemonics, making it easy to monitor program execution.

For designs that use custom or proprietary CPUs, you can use the HP 10320C User-definable Interface to connect the HP 1650A/1651A/16510A to your system. The HP 10391A Inverse Assembler Development Package can be used to develop custom software that converts the acquired state data into your CPU's mnemonics.

View Time-correlated Activity of Two Parts of Your System

The HP 1650A/1651A/16510A can be configured into two independent state analyzers, or one state and one timing analyzer. Measurements that might have required two instruments before can now be made with one instrument.
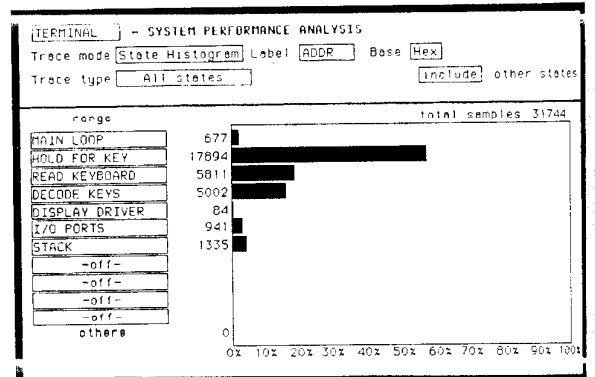
For example, by using the state analyzer to focus on a specific I/O routine, you can watch both the program execution and the activity on the I/O lines with a time correlated display. Or, when you need to examine the interaction of two microprocessors, the HP 1650A/1651A/16510A can display time-correlated state listings.

```
Mixed mode - Display   68000STATE - STATE LISTING
Label  >  ADDR   68000 Mnemonic          Time    R/W
Base   >  Hex    hex                     Rel     Symbol
-0004    008934  BEQ.B  00892E          1.240 us  READ
-0003    008936  CMP.B  #++,D0          1.240 us  READ
-0002    00892C  BCR.B  008920          1.760 us  READ
-0001    008930  B03C unused prefetch   1.240 us  READ
x+0000   0004F4  0000 supr data write   2.000 us  WRITE
0 +0001  0004F6  8930 supr data write   1.480 us  WRITE
+0002    00892A  JMP    0088C6[PC]      1.240 us  READ

68000TIMNG - TIMING WAVEFORMS        X to Trigger  -810.0 ns
Sec/Div [500.0 ns]  Delay [0.000 s]  0 to Trigger  700.0 ns
```

Make simultaneous measurements in both the state and timing domains.

Identify Performance Bottlenecks with System Performance Analysis

The HP 10390A System Performance Analysis software adds three measurements to the HP 1650A/1651A/16510A. The State Histogram and State Overview measurements can display the intensity of activity in specific areas of memory or identify modules that are prime targets for optimization. The Time Interval measurement can be used to measure execution time of a module, time between calls to a module, or time between two different modules.

```
TERMINAL  - SYSTEM PERFORMANCE ANALYSIS
Trace mode [State Histogram] Label [ADDR]  Base [Hex]
Trace type [ All states ]            [Include] other states

   range                                 total samples 31744
MAIN LOOP            677
HOLD FOR KEY       17894
READ KEYBOARD       5811
DECODE KEYS         5002
DISPLAY DRIVER        84
I/O PORTS            941
STACK               1335
  -off-
  -off-
  -off-
  -off-
 others               0
            0%  10% 20% 30% 40% 50% 60% 70% 80% 90% 100%
```

State Histogram ... for characterizing the usage of software modules.

Use Cross-Domain Triggering For Complex Measurements.

Use state to arm timing, or use timing to arm state when the symptom of a problem is best isolated with one analyzer and the cause is best isolated with the other. For example, track a microprocessor's program flow around a hardware interrupt by using the timing analyzer to find the edge of the interrupt signal. Then the timing analyzer can arm the state analyzer to acquire data.

HP 1650A, 1651A, 16510A Specifications

Probes

Minimum Swing: 600 mV peak-to-peak.
Threshold Accuracy: ±150 mV accuracy over the range −2.0 to 2.0 volts; ±300 mV accuracy over the ranges −9.9 to −2.1 volts and 2.1 to 9.9 volts.
Dynamic Range: ±10 volts about the threshold.

State Mode
Clock Repetition Rate: Single phase is 25 MHz maximum. With time or state counting, minimum time between states is 60 ns. Both mixed and demultiplexed clocking use master-slave clock timing; master clock must follow slave clock by at least 10 ns and precede the next slave clock by > 50 ns.
Clock Pulse Width: ≥10 ns at the threshold.
Setup Time: Data must be present prior to clock transition, ≥10 ns.
Hold Time: Data must be present after rising clock transition, 0 ns.

Timing Mode
Minimum Detectable Glitch: 5 ns wide at the threshold.

Characteristics

Probes
Input RC: 100 KΩ ±2% shunted by approximately 8 pF at the probe tip.
Minimum Input Overdrive: 250 mV or 30% of the input amplitude, whichever is greater.
Maximum Voltage: ±40 volts peak.
Threshold Setting: Threshold levels may be defined for pods 1 and 2 individually (HP 1651A). Threshold levels may be defined for pods 1, 2, and 3 on an individual basis and one threshold may be defined for pods 4 and 5 (HP 1650A/16510A).
Threshold Range: −9.9 to +9.9 volts in 0.1 volt increments.

State Analysis
Memory
  Data Acquisition: 1024 samples/channel
Trace Specification
  Clock: Five clocks (HP 1650A/16510A) or two clocks (HP 1651A) are available and can be used by either one or two state analyzers at any time. Clock edges can be ORed together and operate in single phase, two phase demultiplexing, or two phase mixed mode. Clock edge is selectable as positive, negative, or both edges for each clock.
  Clock Qualifier: The high or low level of four clocks (HP 1650A/16510A) or one clock (HP 1651A) can be ANDed with the clock specification. Setup time: 20 ns; hold time: 5 ns.
  Pattern Recognizers: Each recognizer is the AND combination of bit (0, 1, or X) patterns in each label. 8 pattern recognizers are available when one state analyzer is on. 4 are available to each analyzer when two state analyzers are on.
  Range Recognizer: Recognizes data which is numerically between or on two specified patterns (ANDed combination of zeros and/or ones). One range term is available and is assigned to the first state analyzer turned on. The maximum size is 32 bits.
  Qualifier: A user-specified term that can be anystate, nostate, a single pattern recognizer, range recognizer, or logical combination of pattern and range recognizers.
  Sequence Levels: There are 8 levels available to determine the sequence of events required for trigger. The trigger term can occur anywhere in the first 7 sequence levels.
  Branching: Each sequence level has a branching qualifier. When satisfied, the analyzer will restart the sequence or branch to another sequence level.
  Occurrence Counter: Sequence qualifier may be specified to occur up to 65535 times before advancing to the next level.
  Storage Qualification: Each sequence level has a storage qualifier that specifies the states that are to be stored.
  Enable/disable: Defines a window of post-trigger storage. States stored in this window can be qualified.
  Prestore: Stores two qualified states that precede states that are stored.

Tagging
  State Tagging: Counts the number of qualified states between each stored state. Measurement can be shown relative to the previous state or relative to trigger. Maximum count is 4.4×10^{12}.
  Time Tagging: Measures the time between stored states, relative to either the previous state or to the trigger. Maximum time between states is 48 hours. With tagging on, the acquisition memory is halved; minimum time between states is 60ns.
Symbols
  Pattern Symbols: User can define a mnemonic for the specific bit pattern of a label. When data display is SYMBOL, mnemonic is displayed where the bit pattern occurs. Bit patterns can include zeros, ones, and don't cares.
  Range Symbols: User can define a mnemonic covering a range of values. Bit pattern for lower and upper limits must be defined as a pattern of zeros and ones. When data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from base of range.
  Number of Pattern and Range Symbols: 100 per analyzer. Symbols can be down-loaded over RS-232C.

Timing Analysis
Transitional Timing Mode: Sample is stored in acquisition memory only when the data changes. A time tag stored with each sample allows reconstruction of waveform display. Time covered by a full memory acquisition varies with the number of pattern changes in the data.
  Sample Period: 10 ns
  Maximum Time Covered by Data: 5000 seconds
  Minimum Time Covered by Data: 10.24 us
Glitch Capture Mode: Data sample and glitch information is stored every sample period.
  Sample Period: 20 ns to 50 ms in a 1-2-5 sequence dependent on sec/div and delay settings.
  Time Covered by Data: Sample period × 512
Waveform Display
  Accumulate: Waveform display is not erased between successive acquisitions.
  Overlay Mode: Multiple channels can be displayed on one waveform display line. Primary use is to view summary of bus activity.
  Maximum Number of Displayed Waveforms: 24
Time Interval Accuracy
  Sample Period Accuracy: 0.01% of sample period.
  Channel-to-channel Skew: 4 ns typical
  Time Interval Accuracy: ±(sample period + channel-to-channel skew + 0.01% of time interval reading)
Trigger Specification
  Asynchronous Pattern: Trigger on an asynchronous pattern less than or greater than specified duration. Pattern is the logical AND of specified low, high or don't care for each assigned channel. If pattern is valid but duration is invalid, there is a 20 ns reset time before looking for patterns again.
  Greater than Duration: Minimum duration is 30 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Accuracy is +0 ns to −20 ns. Trigger occurs at pattern + duration.
  Less than Duration: Maximum duration is 40 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Pattern must be valid for at least 20 ns. Accuracy is +20 ns to −0 ns. Trigger occurs at the end of the pattern.
  Glitch/Edge Triggering: Trigger on glitch or edge following valid duration of asynchronous pattern and while the pattern is still present. Edge can be specified as rising, falling or either. Less than duration forces glitch and edge triggering off.

Measurement And Display Functions
Autoscale (Timing Analyzer Only): Autoscale searches for and displays channels with activity on the pods assigned to the timing analyzer.

Acquisition Specifications

Arming: Each Analyzer can be armed by the Run key, the other Analyzer, the external trigger in port (HP 1650A/1651A) or the Intermodule Bus (HP 16500A).

Trace Mode: Single mode acquires data once per trace specification; repetitive mode repeats single mode acquisitions until stop is pressed or until time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range. There is only one trace mode when two analyzers are on.

Labels: Channels may be grouped together and given a 6-character name. Up to 20 labels in each analyzer may be assigned with up to 32 channels per label. Primary use is for naming groups of channels such as address, data, and control busses.

Indicators

Activity Indicators: Provided in the Configuration, State Format, and Timing Format menus for identifying high, low, or changing states on the inputs.

Markers: Two markers (X and O) are shown as dashed lines in the display.

Trigger: Displayed as a vertical dashed line in the timing waveform display and as line 0 in the state listing display.

Marker Functions

Time Interval: The X and O markers measure the time interval between one point on a timing waveform and trigger, two points on the same timing waveform, two points on different waveforms, or two states (time tagging on).

Delta States (State Analyzer Only): The X and O markers measure the number of tagged states between one state and trigger, or between two states.

Patterns: The X or O marker can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The O marker can also find the nth occurrence of a pattern before or after the X marker.

Statistics: X to O marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to O time, maximum X to O time, average X to O time, and ratio of valid runs to total runs.

HP 16530A/16531A 400 Megasample/s Digitizing Oscilloscope

Specifications

Vertical (at BNC)
Bandwidth (−3 dB): dc to 100 MHz (dc-coupled)
Range: 40 mV to 16 V full scale (adjustable with 2-digit resolution).
DC Gain Accuracy: ±3% of full scale (valid within ±10°C of auto-calibration temperature)
Analog-to-digital Conversion (ADC) Resolution: ±1.6% of full scale (6 bits)
DC Offset Accuracy: ±1% of offset ±3.2% of full scale (valid within ±10°C of auto-calibration temperature).
DC Offset Range/Resolution:

Vertical Range	Offset Range	Offset Resolution
<800 mV	±800 mV	1 mV
≥800 mV	±16 V	20 mV

Voltage Measurement Accuracy (DC):
Single Cursor (X or O): = Gain accuracy + ADC resolution + offset accuracy.
Dual Cursor (X to O measurements on the same waveform): = Gain accuracy + 2 (ADC resolution)

Horizontal
Range: 50 ns to 100 s full scale, adjustable with 3-digit resolution.
Time Interval Measurement Accuracy (dual channel for deskewed channels with equal rise and fall times):
±0.75 ns ±0.2% of timebase range ±0.02% of reading (2.5 ns sample period)

± sample period ±0.2% of timebase range ±0.02% of reading (≥ 5 ns sample period)

Delay (Time Offset)
Pre-trigger Range: 4096 × sample period
Post-trigger Range: 500 screen diameters
Resolution: Fine adjustment to 0.2% of screen diameter

Characteristics

Vertical
Transition Time (10% to 90%): ≤ 3.5 ns
Input Coupling: dc
Input RC: 1 MΩ ±2% or 50 ohm ±3%, shunted by approximately 13 pF.
Maximum Safe Input Voltage: 1 MΩ input, ±40 V (dc + peak ac), 50 Ω input, ± 5 V (dc + peak ac)
Probe Factors: Any integer ratio from 1:1 to 1:1000, to scale the oscilloscope to represent voltages seen at the probe tip.

Time Base
Deskewing: Skew between channels can be nulled out to compensate for probe cable lengths.

Digitizer
Resolution: 6 bits (1 part in 64)
Digitizing Rate: up to 400 megasamples/second
Digitizing Technique: Real-time digitizing, each 4K record is acquired on a single acquisition.
Acquisition Memory Size: 4096 samples per channel

Waveform Display
Display Formats: Waveforms can be displayed in an overlapping and/or non-overlapping format.
Display Resolution: 500 points horizontally.
Display Modes
Single: New acquisitions replace old acquisitions on screen.
Accumulate: New acquisitions are added to the screen and displayed with older acquisitions until screen is erased.
Average: New acquisitions are averaged with older acquisitions with updated waveform displayed until erased.
Overlay: Up to 8 acquired waveforms can be overlayed in the same display area.
Connect-the-dots: Provides a display of the sample points connected by straight lines.
Waveform Reconstruction: When there is insufficient data to fill every horizontal location, a post-acquisition reconstruction filter fills in the missing locations.
Waveform Math: Display capability of A−B and A+B functions is provided.

Measurement Aids
Markers: Two vertical markers are provided for measurements of time and voltage. Capabilities are: measure voltage of X and O on each analog waveform; measure time from X to trigger, O to trigger, and X to O; automatic marker placement by specifying voltage level, edge number, and rising or falling edge type; run until X to O greater than, less than, in-range, and not-in-range provides selective event search; X to O statistics (mean, max, and min) provide analysis of time interval deviation.
Automatic Measurements: The following pulse parameter measurements can be performed automatically:

Frequency	Rise time	+ pulse width
Period	Fall time	− pulse width
Vpp	Preshoot	$V_{top-base}$
	Overshoot	

Setup Aids
Auto: Auto sets the vertical and horizontal ranges, offset, and trigger level to display the input signals. Requires an amplitude above 10 mV peak, and a frequency between 50 Hz and 100 MHz.
Presets: Scale the vertical range, offset, and trigger level to predetermined values for displaying ECL or TTL waveforms.

LOGIC ANALYZERS

Specifications And Characteristics (cont'd)

Models 1650A, 1651A, 16500A, 16510A, 16515/16A, 16520A/21A 16530A/31A

HP 16515A/16516A 1 GHz Timing Analyzers

Specifications

Probes
Minimum Swing: 600 mV peak-to-peak.
Threshold Range: −3.5 to +5.0 volts in 0.1 volt increments.
Threshold Accuracy: ±125 mV ±2.5%
Dynamic Range: ±7.0 volts

Timing Accuracy
Timing Accuracy: ±1 Sample Period + Sample Rate Accuracy ±(300 ps within a pod, 1 ns between pods)
Sample Rate Accuracy: ±0.01% of measurement added to;
±300 ps at 1 GHz
±400 ps at 250 MHz and 500 MHz
±800 ps at 125 MHz
±1.6 ns at ±62.5 MHz

Characteristics

Probes
Input RC: 50 KΩ ±2% shunted by ≤3 pF at the probe tip.
Minimum Input Overdrive: 250 mV or 25% of the input amplitude, whichever is greater.
Maximum Input Voltage: ±40 volts.

Symbols
Pattern Symbols: User can define a mnemonic covering a range of values. When data display is SYMBOL, mnemonic is displayed where the bit pattern occurs. Bit patterns can include Zeros, Ones, and Don't Cares.
Range Symbols: User can define a mnemonic covering a range of values. Bit pattern for lower and upper limits must be defined as a pattern of Zeros and Ones. When data display is SYMBOL, values within the specified range are displayed as mnemonic ±offset from base of range.
Number of Available Pattern and Range Symbols: 200 symbols can be down-loaded from controller.

Labels: Up to 20 labels may be assigned channels in any configuration up to 32 channels per label. Primary use is for naming groups of channels such as address, data, and control busses.

Indicators
Activity Indicators: Provided in the format menu for identifying high, low, or changing states on the inputs.
Markers: Two markers (X and 0) are shown as dashed lines in the display.
Tracepoint: Displayed as vertical dashed line in the waveform display. Defined as trigger + delay.

Marker Functions
Time Interval: The X and 0 markers measure the time interval between one point on a timing waveform and trigger, two points on the same timing waveform, or two points on different waveforms.
Pattern Search: The X and O marker can be used to locate a specified pattern.
Statistics: X to 0 marker statistics are calculated for repetitive full-memory acquisitions. Pattern must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition (i.e., a hit). Statistics are minimum X to 0 time, maximum X to 0 time, number of hits and number of acquisitions.

HP 16520A/16521A 50 Mbit/s Pattern Generator

Specifications

Clock Sources (16520A Only)
Internal Clock

Clock Period: programmable from 20 ns to 200 μs in a one-two-five sequence.
Data Period Accuracy: ±2% (of period) ±1 ns
External Clock (provided by user)
Input Clock Period: 1 Hz to 50 MHz (20 ns min period) ECL or TTL, internal frequency divide (/1, /5, or /10) provided.
Duty Cycle: 10 ns minimum high time, 10 ns minimum low time
Strobes (16520A Only)
Number of Strobes: 3 (ECL or TTL)
Bits/Channel: 4095
Maximum Bit Rate: 20 MBit/s (50 ns Period)
Edge Placement: ≤10 MBit/s: tenths of period
>10 MBit/s to 20 MBit/s: fifths of Period
(Delay + Width ≤ Period)
Minimum Delay: 0/10 (0/5), maximum delay is 9/10 (4/5) data period.
Minimum Width: 1/10 (1/5) of data period, maximum width is the data period (values in parentheses apply to 20 MBit/s timebase setting). If strobes are desired while operating with external clock. the data rate will be divided to 1/5 or 1/10 the external clock rate.

Characteristics

Output: Eight channel pods can be assigned as either standard ECL or TTL levels. All characteristics are valid at the probe tip.

	ECL	TTL
V$_{OH}$ (steady state) V$_{OL}$ (steady state)	− 0.98V − 1.55V (into 10KΩ, 10 pF)	2.7V 0.6V (into 10KΩ, 10 pF)
Risetime/ Falltime (typ)	2.3 ns (−0.98 V to −1.55 V)	2.5 ns (0.6 V to 2.7 V)
Channel-to- channel Skew* (same card)	≤ 5ns	≤ 5ns
Channel-to- channel Skew* (card-to-card)	< 10ns	< 10ns
Number of Std Loads	3 (10 KH ECL. @ V$_{nh}$=150mV)	3 (LS, @ V$_{nl}$=250mV)

(Output measurements made into a load consisting of 10 KΩ in series shunted with 10 pF to ground.)
(*) Skew measured at (+1.6 V) TTL and (−1.3 V) ECL levels.

DATA CAPACITY	16520A	16521A
Number of Channels	12	48
Bits Per Channel	4095	4095
Maximum Bit Rate	50 MBit/s, 20P (20ns Period)	50 MBit/s, 20P (20ns Period)
INPUT	ECL	TTL
V$_{ih}$ (min)	−0.91V	2.08V
V$_{il}$ (max)	−1.69V	1.12V

Maximum Input Voltage: ±40V

Input Impedance: 100 KΩ, 8 pF

External Clock-in to Clock-out Delay: 50 ns

Data Instruction Set
Break: Stops program execution, last data vector is held at output.
Repeat: Repeats vector up to 256 times.
Wait IMB: Wait for intermodule trigger.
Wait External: Wait for user-defines 3-bit pattern on external input pod to become true. No data cycle latency when pattern is true between 30 ns and 0 ns before next clock edge.

Signal IMB: Arms other measurement cards.

Macro: Four different macros may be defined and inserted as needed. Six character labels may be defined for each macro. Macros contain REPEAT, WAIT EXTERNAL, WAIT IMB, BREAK, and SIGNAL IMB instructions.

General Characteristics

Auxiliary Power Available Through Cables:
HP 1650A/1651A/16510A: ⅔ amp @ 5V per cable; 2 amp @ 5V per HP 1650A/1651A/16510A; 16.3 amp-current draw of installed cards @ 5V per HP 16500A.

Current draw per card (@ 5V): 3.0 amp per HP 16510A, 1.3 amp per HP 16515A, 1.4 amp per HP 16516A, 0.7 amp per HP 16520A, 0.8 amp per HP 16521A, 0.4 amp per HP 16530A, 1.1 amp per HP 16531A.

Programmability: Instrument settings and operating modes, including automatic measurements, may be remotely programmed via RS-232C or HP-IB (IEEE-488). HP-IB is available only on HP 16500A.

Hardcopy Output

Printers Supported: HP ThinkJet, HP QuietJet, HP LaserJet, Epson and Epson-compatible printers (e.g., Epson FX80) via RS-232C or HP-IB (HP 16500A only).

RS-232C Configurations: Protocol: XON/XOFF, Hardware; Data bits: 7, 8; Stop bits: 1, 1½, 2: Parity: none, odd, even; Baud rate: 110, 300, 600, 1200, 2400, 4800, 9600, 19200.

Ordering Information	Price
Logic Analyzers	
HP 1631A (35 channels, plus two analog)	$11,300
HP 1631D (43 channels, plus tow analog)	$13,300
HP 1650A (80 channels)	$7800
HP 1651A (32 channels)	$3900
HP 16500A Logic Analysis System	$7200
HP 16510A (80 channels)	$5200
HP 16515A (16 channels, 1 GHz timing)	$7800
HP 16516A (16 channels, 1 GHz timing)	$6500
HP 16520A (12 channels, pattern generation)	$3700
HP 16521A (48 channels, pattern generation)	$4000
HP 16530A (400 MSa/s oscilloscope timebase)	$1500
HP 16531A (400 MSa/s oscilloscope acquisition)	$4000
Probe Interface	
HP 10269C G.P. Probe Interface	$470
Microprocessor Preprocessors-note, inverse assembly is provided on 3.5-inch disc	
HP 10304B Intel 8085	$880
HP 10305B Intel 8086/88	$1235
HP 10306B Intel 80186/88	$2000
HP 10312D Intel 80286	$2040
HP 10314B Intel 80386	$2200
HP 10307B Motorola 6800/02	$1110
HP 10308B Motorola 6809/09E	$1110
HP 10310B Motorola 68008	$1110
HP 10311B Motorola 68000/10, 64-pin DIP	$1320
HP 10311G Motorola 68000/10, 68-pin PGA	$600
HP 10313G Motorola 68020	$850
HP 10303B National NSC800	$1010
HP 10300B Zilog Z80	$880
Bus Preprocessors	
HP 10342B HP-IB, RS-232C and RS-449	$1220
HP 10342G HP-IB	$350
Minicomputer Interfaces	
HP 10275A PDP-11 UNIBUS**	$470
HP 10276A LSI-11 Q-Bus**	$520
HP 52126A Intel Multibus***	$370
Accessory Software	
HP 10390A System Performance Analysis	$500

User-Definable Interface	
HP 10320C User-definable Interface	$270
HP 10321A Microprocessor Interface Parts Kit	$235
HP 10322A 40-pin DIP Interface Cable	$410
HP 10323A 48-pin DIP Interface Cable	$470
HP 10324A 64-pin DIP Interface Cable	$570
HP 10391A Inverse Assembler Development Package	$1000
Printers and Accessories	
HP 2225A ThinkJet Printer with HP-IB Interface	$...
HP 10833A HP-IB Cable, 1m	$80
HP 2225D ThinkJet Printer with RS-232C Interface	$495
13242-60010 RS-232C Cable	$69
HP 92261A Print Cartridge	$10
HP 92261N Jet Paper (2500 Sheets, fanfold)	$50
HP 92261S Mini-printer Stand	$49
Oscilloscope Accessories	
HP 10503A BNC-to-BNC cable, 1.2m	$20
HP 10017A 10:1, 1 Mohm, 8 pF miniprobe, 1m	$130
HP 10018A 10:1, 1 Mohm, 10 pF miniprobe, 2m	$140
HP 10020A 10:1, 100:1, 10 Mohm, 10 pF resistive divider probe set, 1.5m	$435
HP 10021A 1:1, 36 pF, mini-probe, 1m	$90
HP 10022A 1:1, 62 pF, mini-probe, 2m	$95
HP 10026A 1:1, 50 ohm, mini-probe, 1m	$90
HP 10027A 1:1, 50 ohm, mini-probe, 2m	$95
HP 10032A 100:1, 3 Mohm, 3 pF mini-probe, 1m	$130
HP 10240B BNC-to-BNC AC coupling capacitor	$45
HP 10211A 24-pin IC test clip	$75
Logic Analyzer Accessories	
01650-61607 16-Channel Probe Cable for HP 1650A and HP 1651A	$130
16510-61601 16-Channel Probe Cable for HP 16510A	$160
16515-61602 8-Channel Probe Cable for HP 16515A and HP 16516A	$170
01650-61608 16-Channel Lead Set for HP 1650A, HP 1651A and HP 16510A (grey tip)	$190
16515-62102 8-Channel Lead Set for HP 16515A and HP 16516A (blue tip)	$195
01650-63201 Termination Adaptor for HP 1650A, HP 1651A and HP 16510A	$100
5959-0288 Grabbers (package of 20)	$20
Pattern Generator Accessories	
16520-61601 Input qualifier Probe Cable	$130
16520-61602 8-Channel Data Probe Cable	$165
16520-61603 Clock Probe Cable	$190
HP 10347A Pattern Generator Probe Lead Set	$200
16520-69501 Input Qualifier Probe Kit	$140
HP 10345A 8-Channel ECL Differential Driver Pod	$120
HP 10346A 8-Channel TTL Tristate Buffer Pod	$120
5959-0288 Grabber (package of 20)	$20
Other Accessories	
HP 1008A Option 006 Testmobile	$1240
1540-1066 Soft Carrying Case (for HP 1650A and HP 1651A)	$135
HP 46060A HP Mouse (for 16500A only)	$148
HP 92192A Black double-sided 3.5" microfloppy discs (box of 10)	$55
5061-6175 HP 1650A & HP 1651A Rackmount Kit	$320
5061-9679 HP 16500A Rackmount Kit	$40
9211-2658 HP 16500A Transit Case	$520
9211-2645 HP 1650A & 1651A Transit Case	$430

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